High-Isolation Series-Shunt FET SPDT Switch With a Capacitor Canceling FET Parasitic Inductance

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***Abstract*—A novel series-shunt FET narrow-band high-isolation single-pole double-throw switch, which employs series capacitors to cancel the parasitic inductances has been developed. The proposed switch can have significantly high isolation characteristics at higher frequency. The fabricated two switches have demonstrated high isolation characteristics of 28.9 dB in the 28- and 18-GHz band, respectively.**

***Index Terms*—Microwave switches, monolithic-microwave integrated-circuit switch.**

I. Introduction

SERIES-SHUNT FET single-pole double-throw (SPDT) switches are often used for low-frequency applications (1.9-GHz personal handy-phone system (PHS), etc.) because of their small size and broad bandwidth [1]–[4]. However, they do not have sufficiently high isolation because of FET parasites, especially when they operate in higher frequency range. It is desirable to obtain a high-isolation transmit/receive (T/R) switch for a T/R module. Moreover, a high-isolation switch is important for getting phase shifters with high performance of small gain ripple and low phase error. It is known that an L-FET configuration, which has resonant inductor L connected to an FET in parallel [5], can achieve high isolation at high frequency. However, its bandwidth is restricted because it uses resonance of intrinsic capacitor in an "off" FET and external inductor.

To address these problems for conventional switches, we have proposed a novel series-shunt FET SPDT switch with capacitors canceling parasitic inductor of shunt FETs. The investigation for series-shunt FET switches has shown that degradation of isolation is caused by parasitic inductance of shunt FETs at a high-frequency range. Moreover, it has been demonstrated that a capacitor connected to a shunt FET in series cancels the parasitic inductance and leads to high isolation. The Ka- and K-band series-shunt FET SPDT switches with capacitor canceling parasitic inductor of shunt FETs have been developed and both of them have achieved isolation of 28.9 dB at 28 and 18 GHz, respectively.

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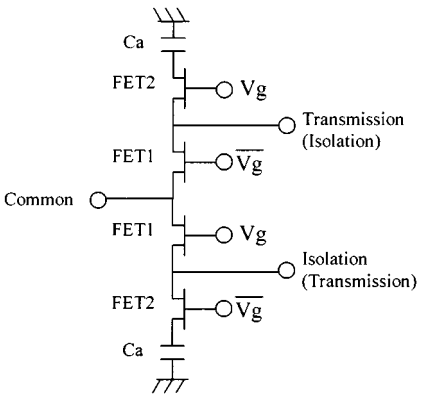


Fig. 1. Circuit scheme of a series-shunt FET SPDT switch with capacitors canceling parasitic inductor of shunt FETs.

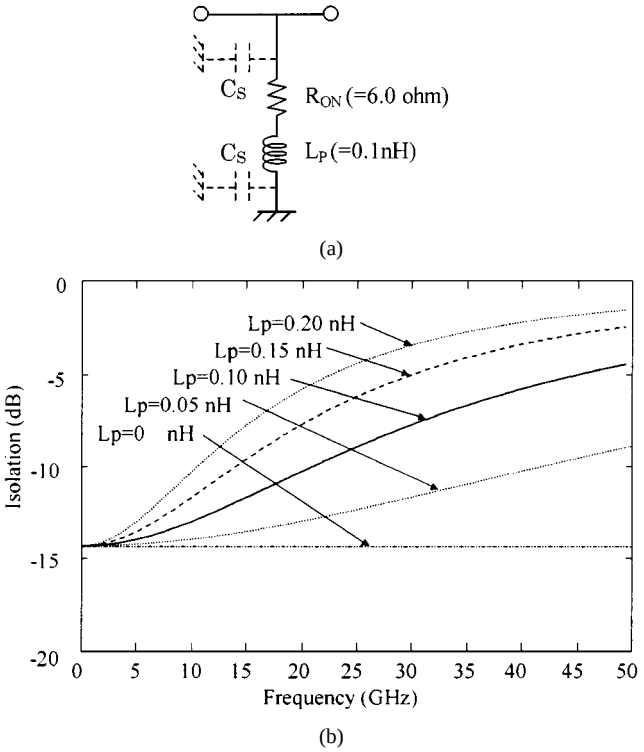


Fig. 2. (a) Simplified equivalent circuit of a shunt FET in the "off" state of the switch. (b) Calculated isolation characteristics of the shunt FET.

II. Series-Shunt FET SPDT Switch With a Capactor Canceling Parastic Inductor

Fig. 1 shows a circuit schematic of the series-shunt FET SPDT switch with capacitors (C_a) canceling parasitic inductor

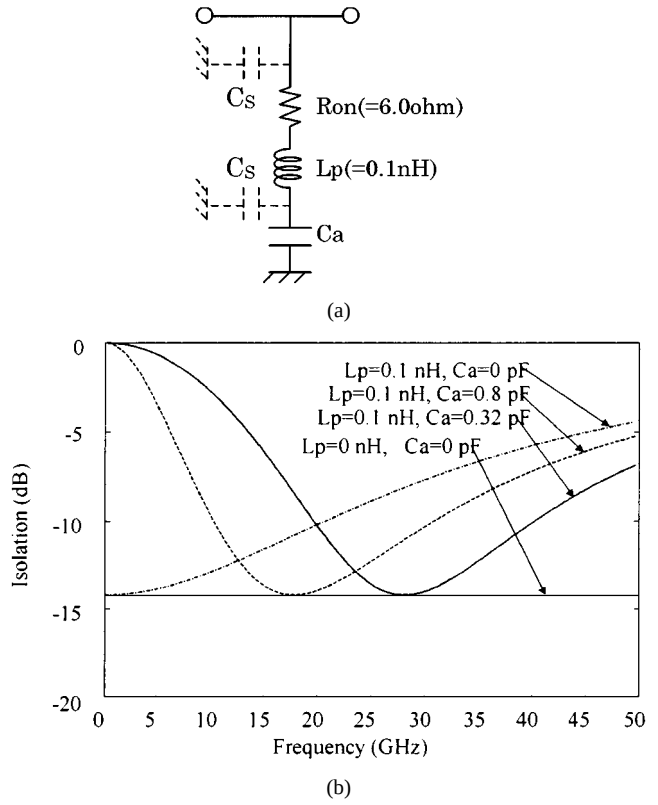


Fig. 3. (a) Simplified equivalent circuit of a shunt FET with series capacitors (C_a) in the "off" state of the switch. (b) Calculated isolation characteristics.

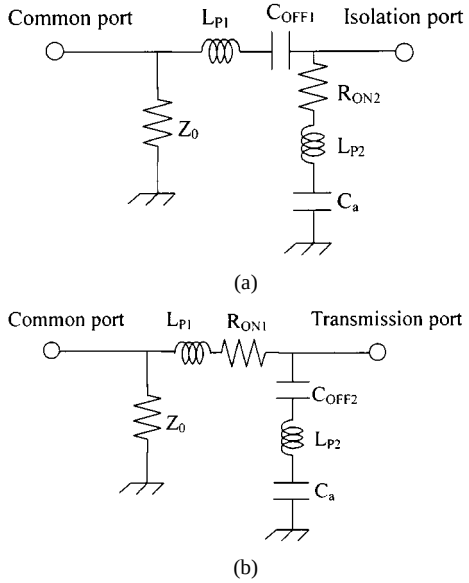


Fig. 4. Simplified equivalent circuit of: (a) isolation port and (b) transmission port of the proposed series-shunt FET SPDT switch with capacitors (C_a) canceling the parasitic inductor L_{p2} of the shunt FET.

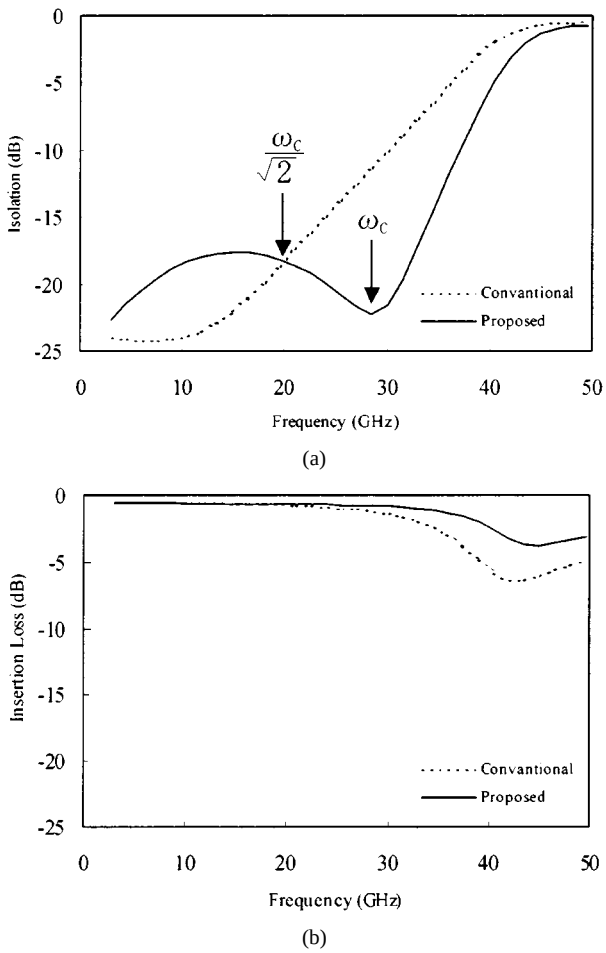


Fig. 5. Calculated: (a) isolation and (b) insertion loss of 28-GHz-band switches with and without capacitors (C_a).

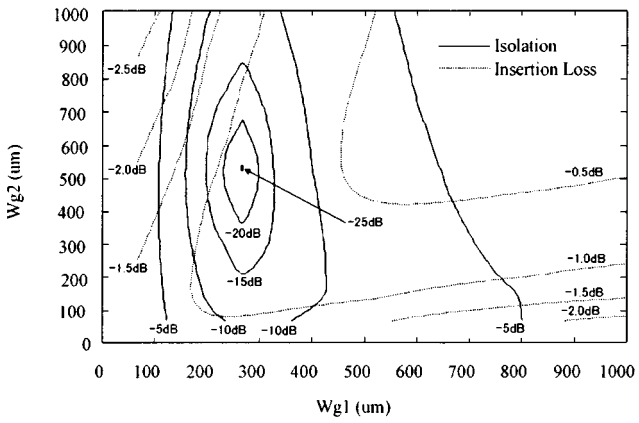


Fig. 6. Calculated contour maps for isolation and insertion loss of the proposed series-shunt FET SPDT switch with capacitors (C_a) at 28 GHz.

of shunt FETs (FET2). In order to obtain high-isolation performance of the switch at high frequency, we have taken an approach to find the cause of the isolation degradation at a higher frequency.

At first, the performance of a shunt FET in the "off" state of the switch is analyzed because the isolation performance of a series-shunt FET SPDT switch highly depends on the isolation of a shunt FET. Fig. 2 shows a simplified equivalent circuit of a shunt FET in the "off" state of the switch and calculated isolation characteristics. Here, the FET's gatewidth is 300 μm. The value of parasitic capacitance ($C_s = 0.0096$ pF) is neglected in the calculation. From Fig. 2, it is illustrated that degradation of isolation of a shunt FET at higher frequency is caused by the parasitic inductor (L_P) of the FET.

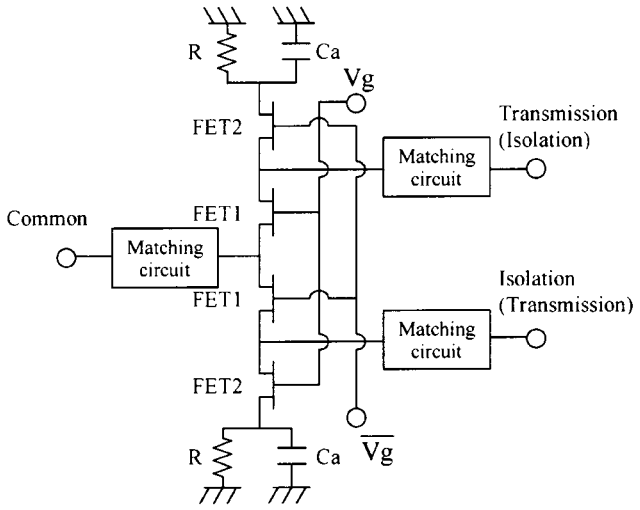
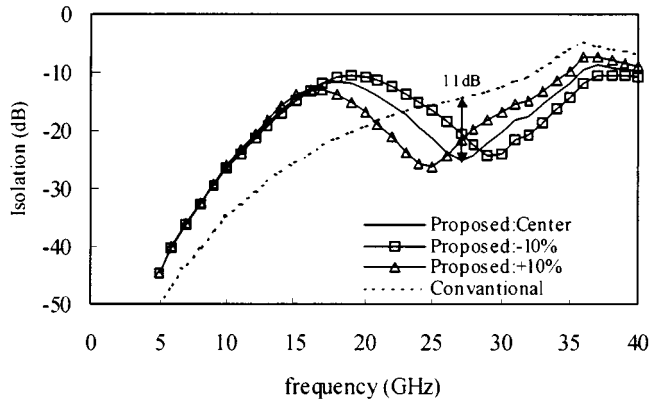
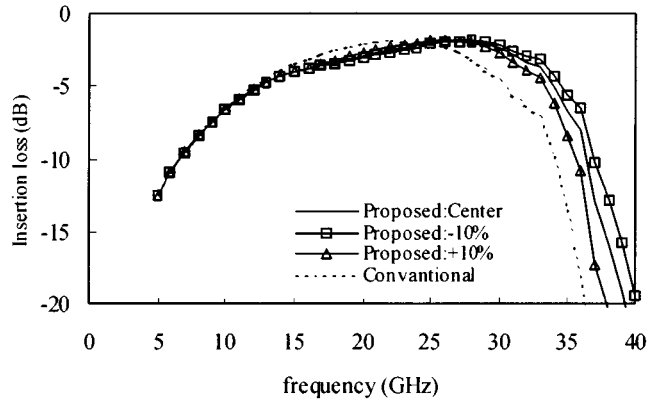


Fig. 7. Schematic diagram of the designed series-shunt FET SPDT switch with capacitors (C_a) canceling the parasitic inductor of the shunt FETs.



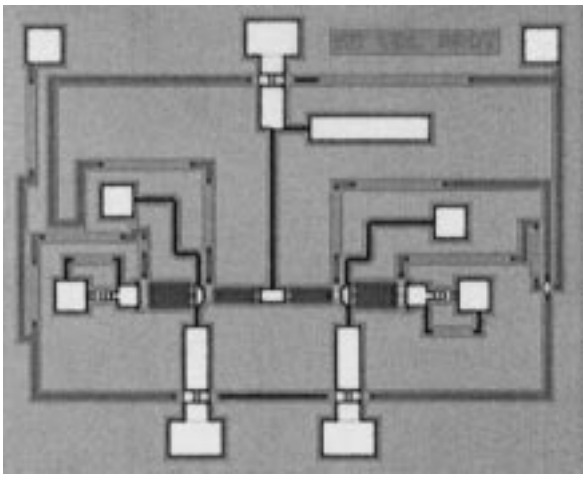
(a)



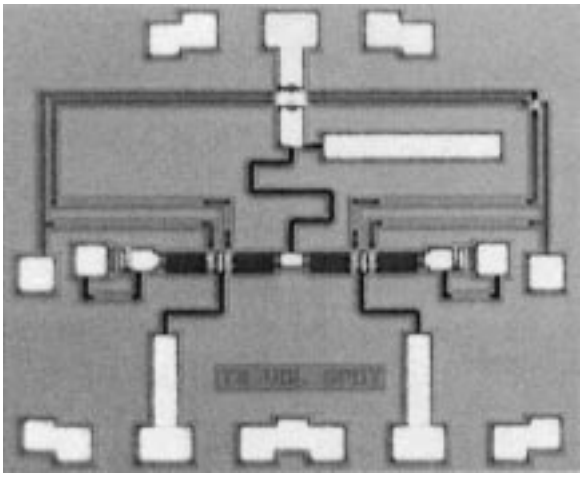
(b)

Fig. 8. Designed and measured characteristics of: (a) isolation and (b) insertion loss for the 28-GHz-band FET SPDT switch with and without capacitors (C_a). The proposed switch is calculated with $\pm -10\%$ shift of metal–insulator–metal (MIM) capacitors.

To cancel out the effect of the parasitic inductor (L_P) of the shunt FET, a capacitor (C_a) is added to the FET in series. The capacitance of the added capacitor C_a should be selected using



(a)



(b)

Fig. 9. FET SPDT switch with capacitors (C_a) designed for the: (a) 28- and (b) 18-GHz band. The chip sizes are 1.63 × 1.34 mm.

the following equation:

$$C_a = \frac{1}{\omega_C^2 L_P} \tag{1}$$

where ω_C is a designed center frequency.

Using (1), the capacitor C_a can be determined optimally according to ω_C.

Fig. 3 shows a simplified equivalent circuit of a shunt FET with series capacitor C_a in the "off" state of the switch and calculated isolation characteristics. The values of C_a are designed so as to realize center frequencies of 28 and 18 GHz. The calculated isolation characteristics have demonstrated the same value of 14.2 dB at both designed center frequencies of 28 and 18 GHz.

Fig. 4(a) and (b) shows the simplified equivalent circuit of isolation port and transmission port, respectively, of the proposed series-shunt FET SPDT switch with the capacitor C_a canceling the parasitic inductor L_{p2} of a shunt FET.

The isolation $S_{21\text{off}}$ of the isolation port and the insertion loss $S_{21\text{on}}$ of the transmission port of the proposed series-shunt FET SPDT switch shown in Fig. 4(a) and (b) can be written as

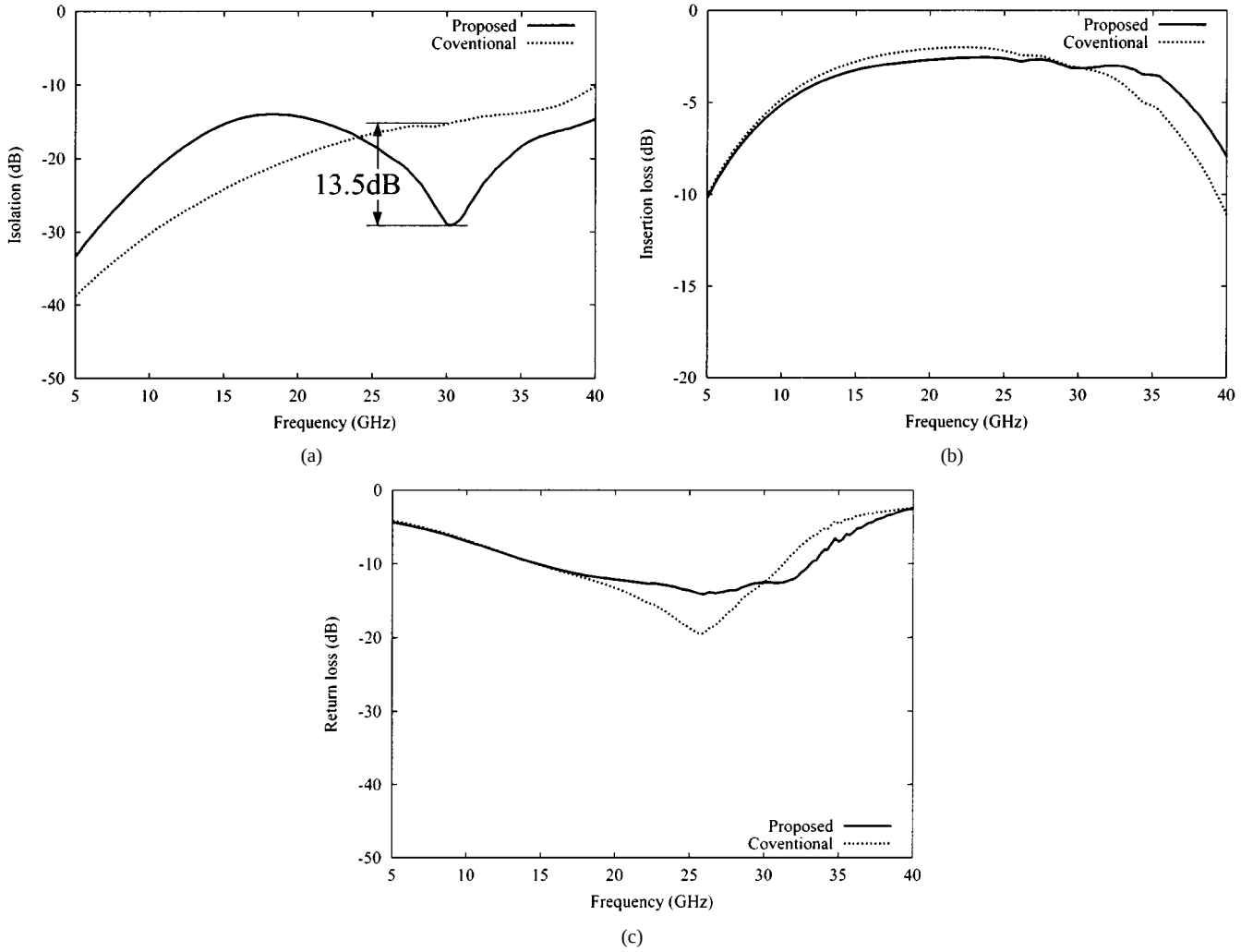


Fig. 10. Measured performances of the 28-GHz-band switch. (a) Isolation. (b) Insertion loss. (c) Input return loss.

follows:

$$
\begin{aligned}
S_{21\text{off}} &= \frac{2}{2+(Y_{2\text{off}}+1)(2Z_{1\text{off}}+1)} \\
Z_{1\text{off}} &= \frac{1}{j\omega C_{\text{OFF1}}} + j\omega L_{P1} \\
Y_{2\text{off}} &= \frac{1}{R_{\text{ON2}} + j\omega L_{P2} + \dfrac{1}{j\omega C_a}}
\end{aligned} \tag{2}
$$

$$
\begin{aligned}
S_{21\text{on}} &= \frac{2}{2+(Y_{2\text{on}}+1)(2Z_{1\text{on}}+1)} \\
Z_{1\text{on}} &= R_{\text{ON1}} + j\omega L_{P1} \\
Y_{2\text{off}} &= \frac{1}{\dfrac{1}{j\omega C_{\text{OFF2}}} + j\omega L_{P2} + \dfrac{1}{j\omega_a}}
\end{aligned} \tag{3}
$$

where R_{ON1} and R_{ON2} are the resistance of the series and shunt FET in the "on" state, C_{OFF1} and C_{OFF2} are the capacitance of the series and shunt FET in the "off" state, and L_{P1} and L_{P2} are the parasitic inductance of the series and shunt FET, respectively. C_a is also derived from the (1). Let C_a be infinite in (2) and (3). The isolation $\overline{S_{21\text{off}}}$ and insertion loss $\overline{S_{21\text{on}}}$ of the conventional series-shunt FET SPDT switch without C_a are then obtained.

From (2), the following relation between $S_{21\text{off}}$ and $\overline{S_{21\text{off}}}$ is derived:

$$
\left|\overline{S_{21\text{off}}}\right| > \left|S_{21\text{off}}\right|, \qquad \text{for } \left(\frac{\omega_C}{\sqrt{2}} < \omega < \infty\right). \tag{4}
$$

With the use of the equivalent circuits shown in Fig. 4, the isolations and insertion losses of the switch with C_a and the switch without C_a can be calculated. Fig. 5(a) and (b) shows an example of calculated isolation and insertion loss, respectively, of 28-GHz-band switches with and without C_a. It can be seen that by adding the capacitor C_a, the isolation and insertion loss of the switch are improved around the designed frequency of ω_C.

When the device parameters of R_{ON1}, R_{ON2}, C_{OFF1}, C_{OFF2}, L_{P1}, and L_{P2} for FET1 and FET2 are substituted into (2) and (3), the isolation and insertion loss for the switch can be calculated. Here, the device parameters are tightly related to the gatewidth W_g of the FET as follows:

$$
\begin{aligned}
C_{\text{off}} &= 1.5 \times 10^{-4} \times W_{g_{(\mu\text{m})}} \text{ pF} \\
L_P &= \frac{30}{W_{g_{(\mu\text{m})}}} \text{ nH} \\
R_{\text{ON}} &= \frac{1800}{W_{g_{(\mu\text{m})}}} \ \Omega.
\end{aligned} \tag{5}
$$

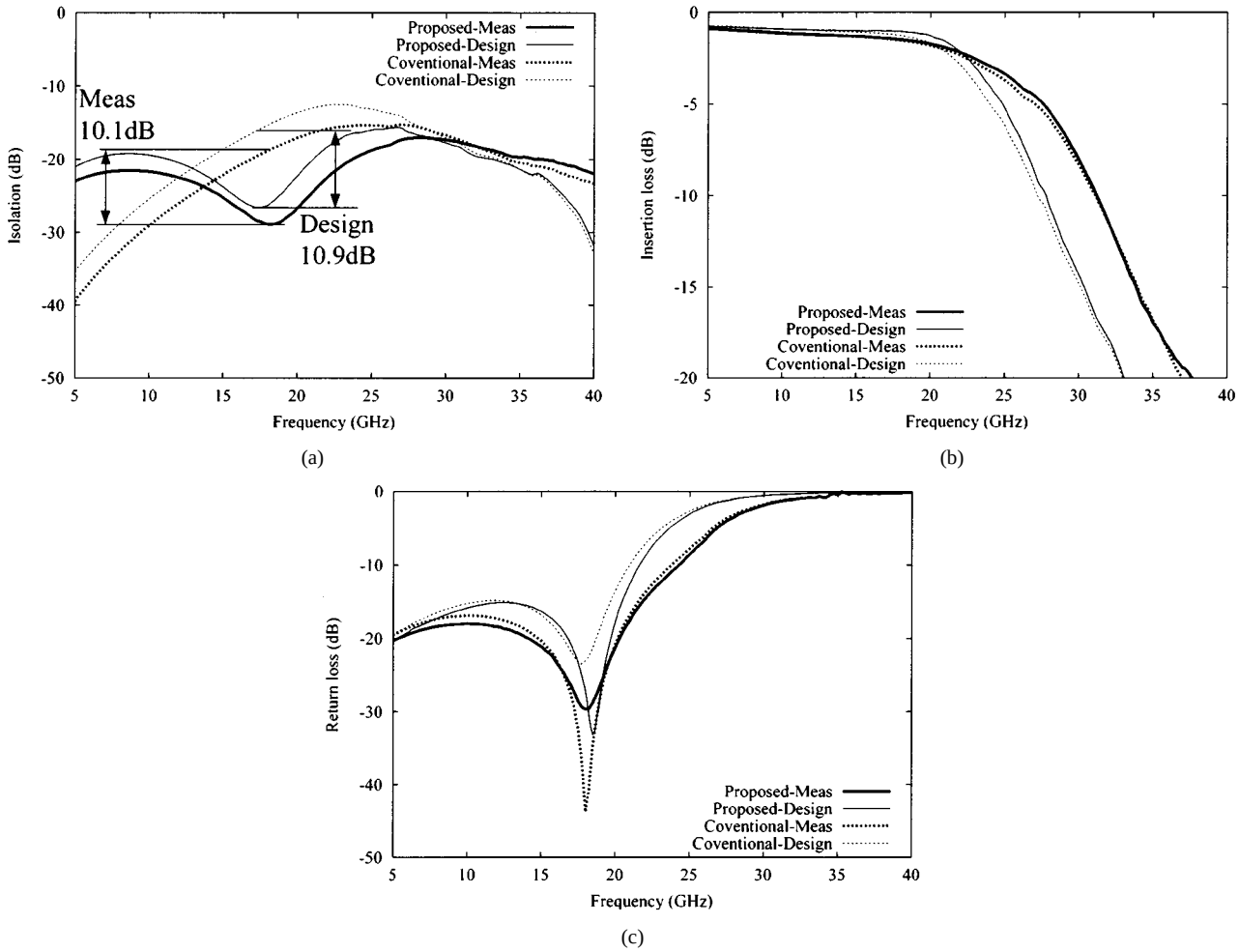


Fig. 11. Designed and measured performances of the 18-GHz-band switches. (a) Isolation. (b) Insertion loss. (c) Input return loss.

Fig. 6 shows the calculated contour maps for isolation and insertion loss of the proposed series-shunt FET SPDT switch with capacitors (C_a) canceling the parasitic inductor of the shunt FETs, which are calculated at 28 GHz. From this figure, it is shown that there exists an optimum pair of the FETs' gatewidth of W_{g1} and W_{g2} for the isolation and insertion-loss characteristics and that the characteristics of the isolation and insertion loss should be traded off.

III. Circuit Design

We have designed the proposed FET SPDT switches for two frequency bands of 28 and 18 GHz. Fig. 7 shows the schematic diagram of the switch. To make a dc return path, R is added in parallel with C_a. In the design procedure, we realize the practical FET model in which all device parameters are related to the gatewidth. Starting from the initial value of W_{g1} and W_{g2} determined by the result of Fig. 6, and utilizing the above-mentioned FET model, we obtain optimized gatewidths.

Fig. 8(a) and (b) shows the isolation and insertion-loss characteristics, respectively, for the 28-GHz-band FET SPDT switch with C_a and without C_a. The gatewidth W_{g1} and W_{g2} are 200 and 400 μm, respectively. The calculated isolation of 24 dB and the insertion loss of 1.9 dB are obtained at 28 GHz for the proposed switch. It is also shown that the isolation and insertion loss of the proposed switch are improved by 11 and 1.1 dB, respectively. For a process with 20% capacitance tolerance, the resonant frequency will shift by $\pm$10%. This causes the 11-dB isolation improvement of the center condition to be reduced to 7 dB. Those are better than the conventional ones at the designed frequency of 28 GHz. It is shown that above the frequency of 22.7 GHz, which corresponds to $\omega_C/\sqrt{2}$, the isolation of the proposed switch is better than that of the conventional one.

IV. Exprimental Results

Fig. 9(a) and (b) shows the FET SPDT switch with C_a designed for the 28- and 18-GHz band, respectively. These chip sizes are 1.63 $\times$ 1.34 mm.

Fig. 10(a)–(c) presents the measured results of the isolation, insertion loss, and return loss, respectively, of the proposed FET SPDT switch with C_a for the 28-GHz band. The switch has demonstrated isolation of 28.9 dB, insertion loss of 3.1 dB, and return loss of 12.5 dB. The isolation is improved by 13.5 dB compared to the conventional ones. Insertion and return losses are almost the same as the conventional ones.

Fig. 11(a)–(c) shows the designed and measured results of the isolation, insertion loss, and return loss, respectively, of the SPDT switch with C_a and without C_a for the 18-GHz band. The gatewidth W_{g1} and W_{g2} are 300 μm. The designed isolation of

26 dB and the insertion loss of 1.0 dB are obtained at 18 GHz for the proposed switch. The switch has demonstrated isolation of 28.9 dB, insertion loss of 1.5 dB, and return loss of 29.6 dB. The designed isolation is improved by 10.9 dB compared to the conventional switch. The measured isolation is also improved by 10.1 dB. Insertion and return loss are almost the same as the conventional ones. From these results, proposed circuit topologies were utilized to realize with high isolation.

V. Conclusions

To achieve high isolation operating in high frequency and a small switch, the series-shunt FET switches with a capacitor canceling parasitic inductance of FET in 28 and 18 GHz have been developed. The isolations are 28.9 dB for both the 28- and 18-GHz FET SPDT switches, respectively. These results have demonstrated that the proposed series-shunt FET SPDT switches with a capacitor canceling FET parasitic inductance would be useful for the operation in millimeter-wave applications.

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